REMARKS

This is in response to the Office Action dated October 1, 2003, claims 1-39 are pending. The Examiner's reconsideration of the objections and rejections is respectfully requested in view of the amendments and remarks.

Claims 9 and 39 have been objected to for an informality. The Examiner stated that the limitation "discarding all out-of state of a processor the system" is not grammatically correct. Claims 9 and 39 have been amended to claim "discarding all out-of-order state." The Examiner's reconsideration of the objection is respectfully requested.

Claims 1, 4, 5, 10-19, 21-31, 34, and 35 have been rejected under 35 U.S.C. 102(b) as being anticipated by Katzman (U.S. Patent No. 3,737,871). The Examiner stated essentially that Katzman teaches all the limitations of claims 1, 4, 5, 10-19, 21-31, 34, and 35.

Claims 1 and 31 claim, *inter alia*, "replacing the stack references with references to processor-internal registers." Claims 12 and 26 claim, *inter alia*, "determining whether a store instruction references a location in a local stack using an architecturally defined register for accessing a stack location, wherein each processor comprises a respective local stack."

Katzman teaches that top of stack register names are assigned according to a unique, predetermined scheme, and each set of names in the scheme is identified as a state (see col. 1 lines 62-65). Katzman does not teach "replacing the stack references with references to processor-internal registers" as claimed in claims 1 and 31, or "determining whether a store instruction references a location in a local stack using an architecturally defined register for accessing a stack location, wherein each processor comprises a respective local stack" as claimed

in claims 12 and 26. Katzman does not teach references to processor-internal registers or local stacks, essentially as claimed in claims 1 and 39, and claims 12 and 26, respectively. Katzman merely teaches memory stacks in core memory and discs having names which are assigned (see col. 1, lines 20-30 and lines 62-65). The memory devices of Katzman, i.e., core memory and discs, are not analogous to processor-internal registers or local stacks. Katzman does not teach the architecture of the CPU, much less that the CPU comprises registers or stacks. Therefore, Katzman does not teach "replacing the stack references with references to processor-internal registers" as claimed in claims 1 and 31, or "determining whether a store instruction references a location in a local stack using an architecturally defined register for accessing a stack location, wherein each processor comprises a respective local stack" as claimed in claims 12 and 26. Therefore, Katzman fails to teach all the limitations of claims 1, 12, 26, and 31.

Claims 4, 5, 10, and 11 depend from claim 1. Claims 13-19 and 21-25 depend from claim 12. Claims 27-30 depend from claim 26. Claims 34 and 35 depend from claims 31. The dependent claims are believed to be allowable for at least the reasons given for the independent claims. Reconsideration of the rejection is respectfully requested. At least claim 18 is believed to be allowable for additional reasons.

Claim 18 recites, *inter alia*, "determining that the rename register does not exist; and performing the load instruction from one of a main memory and a cache of the system."

Katzman teaches a method implementing three registers (see Abstract, col. 2, lines 45-49, and col. 3 lines 5-10). Katzman does not teach an alternative to using the three registers. Katzman does not teach "determining that the rename register does not exist; and performing the load instruction from one of a main memory and a cache of the system" as claimed in claim 18. Katzman's method does not function without the three registers and does not teach performing

the load instruction from one of a main memory and a cache of the system" as claimed in claim 18. Therefore, Katzman fails to teach all the limitations of claim 18. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 2, 3, 32, 33, and 36 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman in view of Morris et al., (U.S. Patent No. 6,286,095). The Examiner stated essentially that the combined teachings of Katzman and Morris teach or suggest all the limitations of claims 2, 3, 32, 33, and 36.

Claims 2 and 3 depend from claim 1, claims 32, 33, and 36 depend from claim 31. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 31. At least claims 3 and 33 are believed to be allowable for additional reasons.

Claims 3 and 33 claim, *inter alia*, "said synchronizing step comprises the step of inserting in-order write operations for all of the stack references that are write stack references."

Katzman teaches that top of stack register names are assigned according to a unique, predetermined scheme, and each set of names in the scheme is identified as a state (see col. 1 lines 62-65). Katzman does not teach inserting in-order write operations for all of the stack references that are write stack references, essentially as claimed in claims 3 and 33. Katzman merely teaches a naming scheme for top of stack registers. Accordingly, Katzman fails to teach or suggest the limitations of claims 3 and 33.

Morris teaches ordered load and store instructions for allowing a programmer to insure particular instructions are executed in a specific order while still allowing the computer to continue executing different types of instructions (see col. 6, lines 49-53). Morris does not teach inserting in-order write operations, essentially as claimed in claims 3 and 33. Morris teaches methods for performing a variety of operations (see col. 6, lines 11-15). However, Morris does

not teach or suggest targeting write stack references, much less, inserting in-order write operations for all of the stack references that are write stack references, essentially as claimed in claims 3 and 33. Therefore, Morris fails to sure the deficiencies of Katzman. The combined teachings of Katzman and Morris fail to teach or suggest all the limitations of claims 3 and 33. Reconsideration of the rejection is respectfully requested.

Claims 6, 8, 9, 20, and 39 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman, in view of Wing (U.S. Patent No. 5,926,832). The Examiner stated essentially that the combined teachings of Katzman and Wing teach or suggest all the limitations of claims 6, 8, 9, 20, and 39.

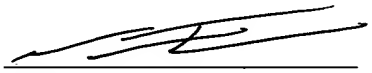
Claims 6, 8, and 9 depend from claim 1. Claim 20 depends from claim 12. Claim 39 depends from claims 31. The dependent claims are believed to be allowable for at least the reasons given for claims 1, 12, and 31. Reconsideration of the rejection is respectfully requested.

Claims 7, 37, and 38 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman, in view of Wing and Morris et al. (U.S. Patent No. 6,286,095). The Examiner stated essentially that the combined teachings of Katzman, Wing, and Morris teach or suggest all the limitations of claims 7, 37, and 38.

Claim 7 depends from claim 1. Claims 37 and 38 depend from claim 31. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 31. Reconsideration of the rejection is respectfully requested.

Accordingly, claims 1-39 are believed to be allowable for at least the reasons stated. The Examiner's withdrawal of the rejections is respectfully requested. For the forgoing reasons, the application is believed to be in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,



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SPECIFICATION (MARKED UP)

METHODS FOR RENAMING ~~STACK REFERENCES~~ A MEMORY REFERENCE TO STACK LOCATIONS IN A COMPUTER PROCESSING SYSTEM